The Science and Technology of Microcalorimeter Arrays

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#### Scope of Talk



- Photon microcalorimeters (with a bias towards x-rays)
- Arrays of independent pixels that do not provide position information on scales finer than the pixel pitch
   Choice for highest spectral resolution
- Means of making electrical contact to the many pixels (but not multi-pixel read-out electronics)
- Design and performance of functioning arrays
   Scale of 32 pixels
- Development of arrays for the future
   Scale of 1024 pixels and greater

# "Single Pixels" to Arrays: Micro-fabrication and Assembly

- Pixel parts: thermometer, absorber, thermal link, electrical contacts
- Pixel size: set by the application, in planar design determines area available for all the pixel parts. Free of this constraint if we can use space out of plane.
- Scale of integration: trade off requirements on yield and uniformity for requirements on precision assembly





## Thermal and electrical view of whole array



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- Pixels in an array share a common heat sink. How solid is How much does its temperature rise when heat from a pixel flows there?
- Need also to consider capacitive or inductive coupling between electrical leads of different pixels, which get pressed closer and closer together with larger arrays.



### Existing, functional arrays: XRS style



- 36-pixel array fully integrated in micro-fabrication except for absorber attachment
- Ion-implanted Si thermistors, Si thermal links, HgTe absorbers
- Operated with 60 mK heat sink
- Two planar formats developed
  - Bilinear: two close-packed rows with thermal links extending outside of active area of the array
  - □ Square: close-packed 6x6 square with weak links of each pixel contained within the unit cell of that pixel 0.64 x 0.64 mm pixels
  - Soft x-ray version of bilinear used in two successful Wisconsin/Goddard sounding rocket experiments
  - □ XRS bilinear launched as part of Astro-E in 2000
  - □ XRS square array to be launched as part of Astro-E2 in 2005
- X-ray astronomy



Suspended thermistors sit over individual DRIE wells in the silicon frame, and the absorbers are attached manually.

#### **XRS heat sinking**

- Chip to alumina board bond made using Stycast 2850:
   90 nW/K with ~ 2 ms equilibration time (due to excess frame heat capacity)



#### Data on XRS-2 square arrays

- Alter 10 10
- 4 arrays completed and tested, resolution 5.3 6.5 eV FWHM with 1-2 outliers per array.
- Crosstalk
  - □ Electrical
    - Seen between nearest and next-nearest neighbors in the feedthroughs to the JFET boxes
    - 0.6% in raw pulse height (nearest neighbors) but 0.1% in optimally filtered pulse height
    - No on-chip electrical crosstalk
  - □ no triggerable thermal crosstalk
    - 0.06% in adjacent pixels seen by averaging (0.015% seen between distant pixels)
    - Noise rather than background
    - Thermal crosstalk and x-rays hitting the frame contribute to a count-rate dependent noise
    - Any energy deposited in the frame (e.g. from a minimum ionizing particle) results in pulses on multiple pixels of scale ~ 3000 less than if the energy had been absorbed directly in a pixel. This scaling derives from the ratio of the pixel G to the chip G.

#### For more details see papers: X04, Y12, Y20, Y21, Y22

#### XRS-2 array: lessons learned



- For the highest resolution at high count rates, need to heat sink the frame better.
- Manual attachment of absorbers still a source of nonuniformity, even with integrated absorber spacers.
   Pulse rise times correlate with baseline resolution.
   Some outliers likely due to attachment or absorber handling. Manual attachment daunting for arrays of much larger scale, though automation might improve reproducibility.

#### Existing functioning arrays: Stanford TES arra



- 6x6 W TES with AI leads, 20 x 20 μm pixels
- Optical spectrometer; energy absorbed in TES directly
- Solid substrate; electron-phonon coupling in W is thermal link
- So far only reading 4 pixels at a time
- 0.15 eV resolution at 1 eV
- Spectro-photometry of compact objects (neutron stars, accreting black holes, white dwarf systems)

#### Stanford TES arrays





#### **Stanford TES arrays**



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### Existing functioning arrays: NIST TES arrays

- 8x8 array of Mo/Cu TES and silicon-nitride membrane thermal links, (ultimately with Bi absorbers), fully integrated in micro-fabrication. 20/64 pixels have electrical leads.
- DRIE wells and surface MEMs versions
- X-ray astronomy and materials analysis (latter doesn't require the fill factor of the former)

#### **NIST TES arrays**





#### 6.4 eV resolution on heat pulses in test array without absorbers

# Existing functioning arrays: SRON TES arrays

- 5x5 array of Ti/Au TES with small Cu absorbers and siliconnitride membrane thermal links, fully integrated in microfabrication
- Si [110] substrate and KOH back etch puts entire row in common substrate trench
- Only 3 pixels wired for independent bias and read-out (central, edge and corner pixel representatives), but the remaining pixels are connected in parallel so that bias power can be applied to the whole chip.
- Best resolution in prototype array 6 eV at 6 keV; the 3 pixels similar

#### **SRON TES arrays**







## Measurement of thermal properties of silicon heat sinks in SRON geometry



- 40 µm wide x 0.4 mm deep Si bars
- 20 mK heat sink
- Comparison of data to modeled profile indicate a phonon mean free path of 150 µm, suggesting cross-over from diffuse to specular transport.
- More accurate measurements are planned

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#### Existing functioning arrays: Goddard TES arra



- 5x5 array of Mo/Au TES using silicon-nitride thermal links and Bi/Cu "mushroom" absorbers, of which a 3x3 subset is wired for read-out and 4 have been operated simultaneously
- The absorber was 4 layers of Bi and 4 layers of Cu. Each Cu layer was 0.2 microns. Each Bi layer was 2.25 or 2.0 microns, for a total of 8.5 microns of Bi.
- Best pixel:
  - □ 5.5 eV at 1.5 keV
  - □ 7.0 eV at 5.9 keV



#### **GSFC TES arrays: crosstalk**

- System not designed for low electrical crosstalk
- Thermal crosstalk distinguished by reversing polarity of bias.
- Nearest neighbor thermal crosstalk about 0.1%
- Diagonal neighbor thermal crosstalk ~10 times lower
- Preliminary determination of heatsinking G at 0.1 K ~ 60 nW/K. Au heat sinking bonds included but insufficient.
- More measurements needed



Advantage of extreme electro-thermal feedback: only a small fraction of the photon energy flows to the heatsink. The rest is compensated by the reduction in Joule power. <sup>20</sup>

#### Arrays of the future



- X-ray astronomy the biggest driver
  - □ XEUS, Constellation-X, and NeXT
  - Each 32x32 arrays; 0.25 mm pixels for XEUS and Con-X, larger for NeXT
  - □ Close packing needed for adequate effective area and image sampling
  - □ Larger arrays would provide increase in focal plane coverage
- Technical challenges of these arrays
  - □ Fabrication and assembly
  - □ Uniformity and yield
  - □ Thermal and electrical contacts
  - □ Thermal and electrical crosstalk

Full integration vs. modularity

#### **Building arrays from modules**



- Allows pre-screening smaller segments, for potentially higher yield
- Natural assembly layers provide ample room for contacts
- Potentially can remain modular after integration, but difficult in practice, especially with tight tolerances on alignment
- Heat sinking the multiple components more complex
- Electrical contacts at the end of the array more complex







#### **Vertical modules**



GSFC SHARC II bolometer array of folded rows of pixels





#### Concept for x-ray version



SAO concept for Con-X, integrated from sub-pixel components

#### Horizontal modules





One SRON concept for XEUS, mainly to lessen wire density

A variety of other stacked arrays have been proposed, e.g. for magnetic calorimeters (Brown/Heidelberg).



# Fully monolithic arrays with high-density contacts



GSFC, SRON, NIST have similar "bulk micromachining" concepts for TES arrays

- Each group presently making and operating small arrays using this technique
- SRON: anisotropic wet etchant cuts trenches in <110> Si
- NIST, GSFC: deep RIE cuts individual wells in <100> Si
- With fine line lithography it should be possible to bring out all the leads on the surface between pixels in a 32x32 array
- Japanese TES collaboration also developing arrays of this scheme and have successfully demonstrated components of it LTD-10, Genoa, 7-11 July 2003

## Fully monolithic arrays with high-density contacts



GSFC developing ultra-low-resistance through-wafer micro-vias for bringing contacts to the backside of a wafer, where they can be bump-bonded to a fan-out board that connects to (or possibly incorporates) the first stage of the read-out. The fan-out board could be designed with multiple contact layers. Electroplating of both Cu and Al is being developed. For Cu, filled vias are needed to keep the series resistance low, but superconducting Al need only be a coating. Japanese TES collaboration has successfully fabricated Sn/Cu micro-via test structures.



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- NIST and SRON developing "surface micromachining" process for bringing contacts out under the pixels.
- NIST approach raises the pixel membranes above the wafer surface
- SRON approach uses a buried wiring layer, leaving pixel membranes in plane of wafer surface
- Issue of "print-through" of wiring layer features in the nitride and TES. If it adversely affects performance, planarization may be required.

#### **Electrical cross talk issues**



SRON modeling led to the conclusion that magnetic screening is necessary, either through use of a separate micro-stripline per channel or a common ground plane close beneath the lines.



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#### Magnetic field & inductance simulation

**Parallel lines** 

**Microstrip lines** 

#### **Thermal design issues**



- For TES arrays, minimizing thermal crosstalk is aided by extreme electrothermal feedback, which offsets most of the input energy of a photon by reducing the Joule power into the TES.
- The thermal design of a 1000-pixel TES array will be driven instead by the integrated bias power. At typically >10 pW/pixel, array heat sinks will need much higher thermal conductance than presently obtained to keep the whole die from heating and to keep each pixel connected to the same reference temperature. The SCUBA 2 monolithic TES bolometer array, which is the first such array to deal with high power loads, is heat sunk through its indium bump bonds.

#### **Microcalorimeter arrays: conclusions**



- We are well into the era of small (30-pixel) microcalorimeter arrays with the era of small (30-pixel) microcalorimetera of small (30-pixel) microcalorimeter array
- Techniques and processes needed for 1000-pixel arrays are being developed and proven in smaller arrays
- Electrical and thermal models of the entire array system (frame, mounting substrate, interconnects) are required for optimal performance of the array as a whole. Measurements and simulations of electrical cross talk and heat sinking being done now are critical to the design of future large scale arrays. Put heaters and diagnostic thermometers on your next array layouts!
- There is no fixed scale cut-off. High-density interconnects remain a challenge for large arrays, particularly of small (<0.25 mm) pixels. Surface wiring eventually becomes infeasible with increasing scale, but the development of vias and multi-layer wiring could make arrays > 1000 pixels possible
- At LTD-11, expect reports of results from 32x32 arrays!